Course Name: Computer Architecture

Course Code: COMP 452	**Course Type: Elective**	**Course Credits: 3**
Class Timings: TBD	**Section: A and B**	**Student Meeting Hours/ Office Hours:** TBD

Instructor Name: Dr. Muhammad Haroon Shakeel

A Note from the Instructor:

- All lectures and related material will be uploaded on Moodle and Google drive weekly.
- Assignments / home works will be uploaded on Moodle and students will submit them in class.
- All emails regarding the course should be sent through official FCC student email account and should have subject line starting as "COMP 452 "

Instructor Contact Details

Email: muhammadharoon@fccollege.edu.pk
WhatsApp Group: TBD
Office Hours: MWF 1200-1400
Guidelines for contacting instructor: you can appointment for some other day via email

Course Description:
Pre-requisites if any: COMP 301
The course provides an understanding of design issues of computer systems from the perspective of performance measures and cost-performance tradeoffs. The course covers fundamentals of modern computer design. Topics include instruction set design, RISC vs. CISC architectures, memory management, caches, memory hierarchies, pipelining, parallelism and multiprocessor systems.

Main Mode of Instruction: In person
Technology Requirements Check Moodle on daily basis, internet is required to access material**.**
Considerations for Students with Limited Internet/Technology Access: Obtain course material in office hours. Announcements for the quizzes will also be made during the class so catch up if you miss any class.

Course TA: NA

Course Objectives or Student Learning Outcomes (SLOs)

a) To provide understanding of basic designs of fundamental computing components.
b) To familiarize students with combinational and sequential circuits
c) To introduce Arithmetic Logic Unit design along with 1 bit and 32 bit adder.
d) To describe the performance evaluation criteria of computers and compare different advanced computing systems.
e) To describe Instruction Set Architecture and single cycle CPU
f) To describe design concepts of modern computer architecture such as pipelining, dynamic branch prediction, dynamic scheduling, loop unrolling
g) To describe existing bottlenecks in computer architecture designs such as control and data hazards, inefficient memory hierarchy and suggest potential solutions

h) To describe the concepts of virtual memory and analyze its contribution towards performance improvement of a computing machine

Course Content, Learning Material & Activities Schedule

WEEK	TOPICS	READING
1.	1. Introduction to CA, its applications and fundamentals **a. Introduction and applications of CA** **b. Von Neumann Architecture** **c. Decoders, Multiplexers, Encoders, Truth Tables**	Ch. B.1, B.2
2-4.	2. Basic Circuits Designs **a. 1-bit ALU, 32-bit ALU** **b. Combinational Circuits, Sequential Circuits** **c. Latches, Flip-Flops, Registers, Finite State Machines** **c. Performance Measures, Power VS Performance** **d. Performance Evaluation Criteria, CPI, Clock Rate, Amdahl's law**	Ch. B.3, B.5, B.1-B.10 Ch. 1.6, 1.10
5.	3. Instruction Set Architecture **a. Introduction to Instruction Set Architecture (ISA)** **b. Categories of ISA** **c. Performance Enhancement Approaches (CPI Improvements) and their comparison**	Ch. 2.5, 2.10
6-7	4. Pipelined Processor **a. Single Cycle Datapath** **b. Pipelining Basics** **c. ALU Controller, Main Controller Design** **d. MIPS 5-stage pipeline**	Ch. 4.1-4.4
8	5. Pipelining Hazards **a. Structural Hazards**	Ch.4.5-4.6

	b. Data Hazards **c. Control Hazards**	
9	**Midterm Exam**	
10	6. Removing Hazards and Branch Predictions **a. Static Branch Prediction** **b. 2-bit Branch Predictor** **c. Dynamic Branch Prediction** **d. Data Forwarding**	4.7-4.8
11-12	7. Instruction Level Parallelism **a. Loop Unrolling** **b. Scoreboarding** **c. Tomasulo's Approach**	4.10
13	8. Cache **a. Estimating Cache Size** **b. Handling Cache Misses and Writes** **c. Cache Performance improvement methods**	Ch. 5.2-5.4
14	9. Virtual Memory Management and Paging **a. Handling Page Faults** **b. Page Writing Schemes** **c. Improving Performance with Translation Lookaside Buffer (TLB)** **d. Handling TLB misses and page faults** **e. Cache coherence and cache protocols**	Ch. 5.7-5.10
14	10. Virtualization and Cloud Computing **a. Virtualization** **b. Hypervisor** **c. Type 1 and Type 2 Virtualization** **d. Current hardware trends**	Handouts
16	**Final Exam**	

'Out-of-class' Study Required:

- See lecture slides before the class
- Check Moodle and your course WhatsApp group regularly
- At least spend 3 hours at home for reading from book
- Do all assignments and homeworks yourself

Textbooks, Materials, Supplies, and other Resources

Textbook: (T1) Computer Organization and Design, 5th edition, David A. Patterson, John L. Hennessy

Reference Books: (T2) Computer Architecture: A Quantitative Approach, 6th edition, John L. Hennessy, David A. Patterson

The books will be uploaded on Moodle.

Course Requirements:

Class Participation

Attend the lectures and participate in discussions. Ask questions and try to answer the questions (even if the answer is wrong)

Assignment 1

Will be focused on fundamental performance metrics of CPUs and performance comparisons. Furthermore, 5-stage MIPS pipeline will be part of the first assignment.

Assignment 2

Will be focused on multi-cycle pipeline, scoreboard, and tomasulo's hardware.

Tests & Quizzes

There would be 5 quizzes, with N–1 policy. Majority of the quizzes would be announced. Check lecture slides for such announcements.

The breakup is as follows:

Class Participation	10%
Assignments:	10%
Quizzes:	20%
Midterm exam:	25%
Final term exam:	35%
TOTAL	**100%**

Missed Assignments/ Make-Ups/ Extra Credit

- *Exam retakes will only be allowed in exceptional circumstances with prior approval.*
- No retake of quizzes, unless approved.

Attendance Policy:

-*You are encouraged to attend all lectures. Students will be responsible to catch up with any missed announcement/lecture/content.*

Classroom Participation:

-*Participate in the class discussions. Try to ask relevant questions and clear doubts within class. Its okay to answer wrongly.*

Grade Determination & Course Assessment as per FCC Policy:

- *Relative grading policy will be adapted*
- *20% penalty per day will be imposed on late assignment submissions*
- *0 credit will be given for plagiarized submissions.*

Changes to the Syllabus:

This syllabus was designed to convey course information and requirements as accurately as possible. It is important to note however that it **may** be subject to change during the course depending on the needs of the class and other situational factors. Such changes would be for your benefit and you will be notified of them as soon as possible.

Student Support Services

Student Counseling Services.Students can contact the Campus Counseling Center at 0331-444-1518 or email ccc@fccollege.edu.pk.
Writing Center
Mercy Health Center

Other Useful FCCU Policy Documents:

Sexual Harassment Policy
Anti-Corruption Policy
Academic integrity

Plagiarism Policy
Academic Calendar