



## FORMAN CHRISTIAN COLLEGE (A Chartered University)

Spring 2023

COMP 300 – Computer Organization and Assembly Language

(3 Credit Hours) Section – A and B

Course Outline and Lesson Plan

### Instructor Information:

Name: Dr. Ayesha Khan

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Office Hours: Wednesday 8am to 9am

Friday 10am to 1 pm

### NOTE:

- There will be **no retake for the quiz**.
- **Students are advised to attend all lectures**. It is entirely the students' responsibility to recover any information or announcements presented in lectures from which they were absent.
- **All work** that you submit in this course **must be your own**.
- **Unauthorized group efforts** are considered academic dishonesty.
- **Cheating, plagiarism and other forms of academic fraud** are taken very seriously. University Policy of plagiarism will be applicable.
- **Cheating or violation of academic integrity in any exam will result in an 'F' grade.**

Course Code: COMP300

Course Title: Computer Organization and Assembly Language

### Catalog Description:

Computer Organization and Assembly Language is offered as a core course for BS degree in Computer Science. This course introduces the organization of computer systems and usage of assembly language. The architecture being followed is MIPS. The students should have prior knowledge of any programming language and Digital Logic. It's a 2+2 credit hour course that includes lab. T

### Grading Policy:

Final	35%
Midterm	20%
Assignments	10%
Quizzes	15%
Lab	15%
Class Activities	5%



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<b>Course Objective(s)</b>	<b>Course Outcome(s)</b>	<b>Assessment(s)</b>
<ul style="list-style-type: none"> <li>Identify the major components of computer architecture, and explain their purposes and interactions.</li> <li>Simulate the internal representation of data, and show how data is stored and accessed in memory.</li> <li>Explain the relationships between hardware architecture and its instruction set, and simulate micro-programs.</li> <li>Explain the Instruction Execution Cycle.</li> <li>Explain the differences and relationships among high-level, assembly, and machine languages.</li> <li>Write well-modularized computer programs in an assembly language, implementing decision, repetition, and procedure structures.</li> <li>Write moderately complex assembly language subroutines</li> </ul>	<ul style="list-style-type: none"> <li>Understand the basic organization of a Conceptual Computer</li> <li>Understand the organization MIPS architecture</li> <li>Ability to design programs with Interactive Input and Output</li> <li>Ability to design programs utilizing arithmetic and logical expressions</li> <li>Ability to design programs utilizing Program Transfer Instructions and Stack Memory Addressing Instructions</li> <li>Ability to design programs utilizing Conditional Program Transfer Instructions</li> <li>Ability to design programs utilizing Stack</li> <li>Ability to design programs utilizing procedure</li> <li>Ability to design program Control Structures using Conditional Jumps</li> <li>Understand the enhancements that can be added in an architecture such as Pipelining, Cache and Virtual Memory</li> </ul>	<p>Quizzes                    15%</p> <p>Assignment                10%</p> <p>Midterm Exam            25%</p> <p>Final Exam                35%</p> <p>Lab Work                    15%</p>



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**Textbooks and References:**

<b>Textbook Name + Edition</b>	<b>Author</b>	<b>Publisher</b>
Computer Organization and Design; The Hardware / Software Interface 5 <sup>th</sup> Edition	David A. Patterson John L. Hennessy	Morgan Kaufmann
Introduction to MIPS Assembly Language Programming 2 <sup>nd</sup> Edition	<i>Charles W. Kann</i>	Charles W. Kann III

**Syllabus breakdown in lectures:**

<b>Week no.</b>	<b>Topic</b>	<b>Content Breakdown</b>
1	Why Computer Organization	<ul style="list-style-type: none"><li>○ Power Trends</li><li>○ Moore’s Law</li><li>○ Power Equation</li></ul>
2	Introduction to Logic Design	<ul style="list-style-type: none"><li>○ Binary Numbers</li><li>○ Decoders</li><li>○ MUXs</li><li>○ Flips Flops</li><li>○ Memory (RAM) Design</li><li>○ Data Bus Design</li><li>○ Registers</li></ul>
3	Design of ALU	<ul style="list-style-type: none"><li>○ Adder circuit in conjunction with MUXs and logic gates to implement arithmetic and logic operations</li></ul>
4-5	MIPS	<ul style="list-style-type: none"><li>○ Introduction to MARS(MIPS Assembler and Runtime Simulator) environment</li><li>○ Hello World program in MIPS (<b>Microprocessor without Interlocked Pipeline Stages</b>)</li></ul>

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		<ul style="list-style-type: none"><li>○ Reading integers, characters, strings and floats</li><li>○ Arithmetic and Logic Operators in MIPS</li><li>○ Instruction types and its format in MIPS</li><li>○ Translating assembly language into machine code.</li></ul>
6-7	Design and Implementation of a Single Cycle MIPS Processor	<ul style="list-style-type: none"><li>○ Von Neumann Vs Harvard Architecture</li><li>○ Data and Code Memories</li><li>○ Fetching an instruction</li><li>○ Execution of R-type and I-Type instructions.</li><li>○ Execution of a branch instruction.</li><li>○ The complete single cycle data path.</li></ul>
8-10	Programming in MIPS	<ul style="list-style-type: none"><li>○ Functions without any input parameters and return values.</li><li>○ Functions with input parameters only.</li><li>○ Functions with return values only.</li><li>○ Functions with both input parameters and return values.</li><li>○ Accessing memory in MIPS</li><li>○ Register offset access</li><li>○ Control Structures and Loops in MIPS</li><li>○ Arrays in MIPS</li><li>○ Stack data structure</li></ul>
11-12	Pipelining	<ul style="list-style-type: none"><li>○ Five Phases</li><li>○ Making 5-stage pipeline work</li><li>○ Pipeline performance</li><li>○ Pipeline data path</li><li>○ Datapath and Control Signals</li><li>○ Pipeline Hazard</li></ul>
13-14	Cache	<ul style="list-style-type: none"><li>○ Introduction</li><li>○ Principle of Locality</li><li>○ Cache Design</li><li>○ Direct Mapped Cache</li><li>○ Associativity</li></ul>



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15	Introduction to Virtual memory (Optional)	<ul style="list-style-type: none"><li>○ Cache miss and page fault</li><li>○ The page table</li><li>○ Translation Look aside Buffers (TLBs)</li></ul>
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